SONY

Diagonal 4.0 mm (Type 1/4.5) 640 × 480 CMOS Image Sensor with Square Pixel for ToF Cameras

IMX570PLR-C

General Description and Application

The IMX570PLR-C is a diagonal 4.0 mm (Type 1/4.5) 640 × 480 fully integrated ToF (Time-of-Flight) camera sensor which allows to address 3D applications such as gesture recognition, active controls, real world acquisition. It is specifically designed for FA / Security. The sensor implements DepthSense™ pixel technology. When used in combination with a pulsed IR light source, this sensor can return correlation data, from which depth and confidence images at 640 × 480 resolution can be derived. It contains an integrated illumination controller and can be configured and controlled through an SPI Interface. It operates with analog 2.7 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption.
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Functions and Features

- Back-illuminated Time-of-Flight image sensor
- High signal to noise ratio (SNR)
- 1/4.5-type optical Time-of-Flight sensor (optical area 3.2 × 2.4 mm^2)
- 5 × 5 μm^2 pixels
- 640 × 480 DepthSense™ Time-of-Flight pixels
- Full resolution @max56 frame/s (4phase/frame)
- Pixel binning readout function
- Independent flipping and mirroring
- CSI-2 serial data output (MIPI 2lane, 1440 Mbps/lane, D-PHY spec. ver. 1.2 compliant)
- I2C serial communication (Supports I2C "Fast-mode" / "Fast-mode Plus")
- SPI Master for peripheral configuration
- Demodulation frequency up to 120 MHz
- Shutter feature embedded
- 192 bits of OTP for users
- Built-in temperature sensor

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E21106

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Device Structure

Time-of-Flight Image Sensor

Image size	: Diagonal 4.0 mm (Type 1/4.5)
Number of effective pixels	: 648 (H) × 488 (V) approx. 0.316 M pixels
Number of active pixels	: 640 (H) × 480 (V) approx. 0.307 M pixels
Package size	: 9.50 mm (H) × 8.70 mm (V)
Unit cell size	: 5 µm (H) × 5 µm (V)
Substrate material	: Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Supply voltage (analog)	VANA	-0.3 to +3.3	V	Refer to VSS level
Supply voltage (mix)	VMIX	-0.3 to +1.8	V	
Supply voltage (digital)	VDIG	-0.3 to +1.8	V	
Supply voltage (interface)	VIF	-0.3 to +3.3	V	
Input voltage (digital)	VI	-0.3 to +3.3	V	
Output voltage (digital)	VO	-0.3 to +3.3	V	
Guaranteed Operating temperature	T_{opr}	-30 to +75	˚C	
Guaranteed storage temperature	T_{stg}	-40 to +85	˚C	
Guaranteed performance temperature	T_{spec}	-10 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	Notes
Supply voltage (analog)	VANA	2.6	2.7	2.9	V		Refer to VSS level
Supply voltage (mix)	VMIX	0.79*	1.2	1.3	V	*Refer to 18-1	
Supply voltage (digital)	VDIG	1.1	1.2	1.3	V		
Supply voltage (interface)	VIF	1.7	1.8	1.9	V		

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PKG Center and Optical Center (Top View)

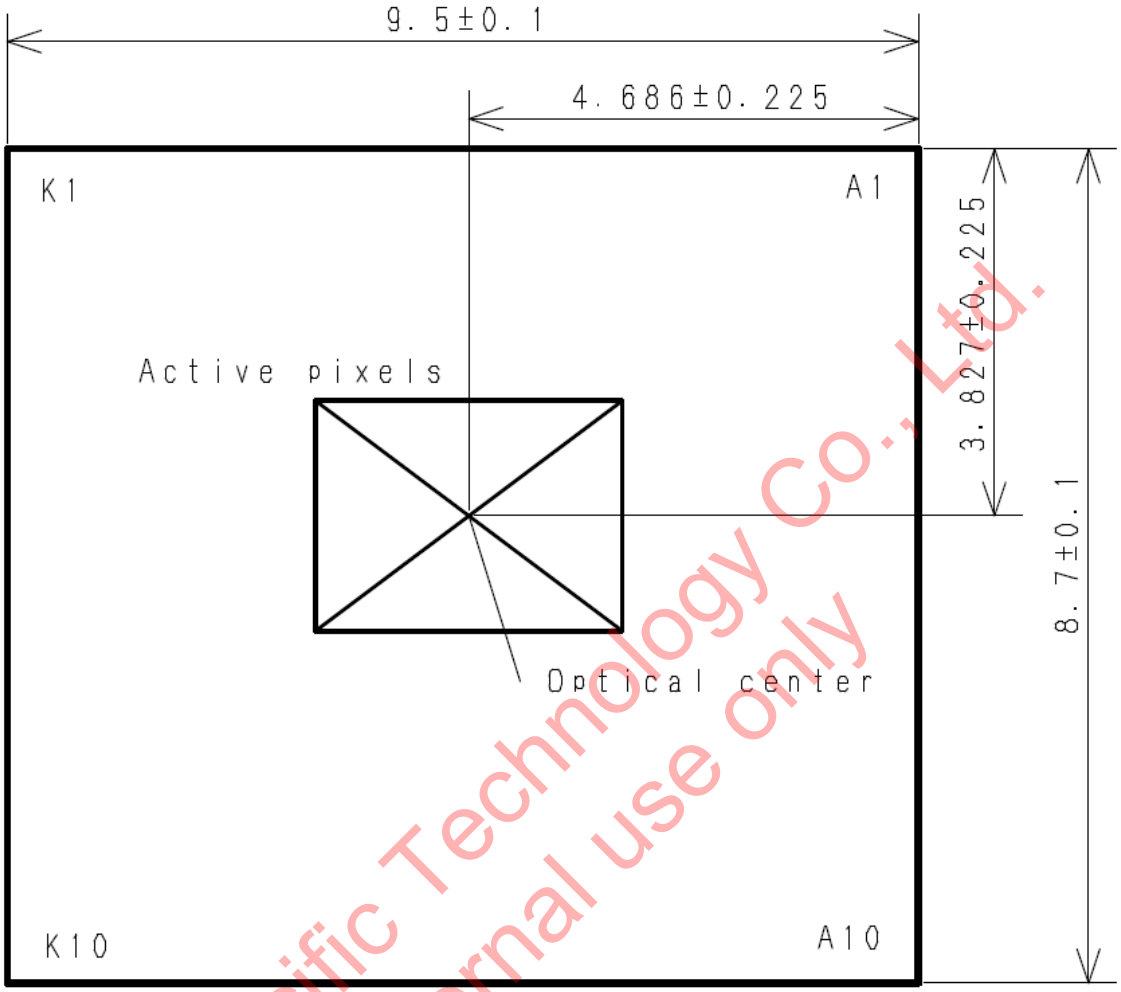

Figure 1 PKG Center and Optical Center (Top View) (x and y coordinates in mm)

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1. Pin Coordinates

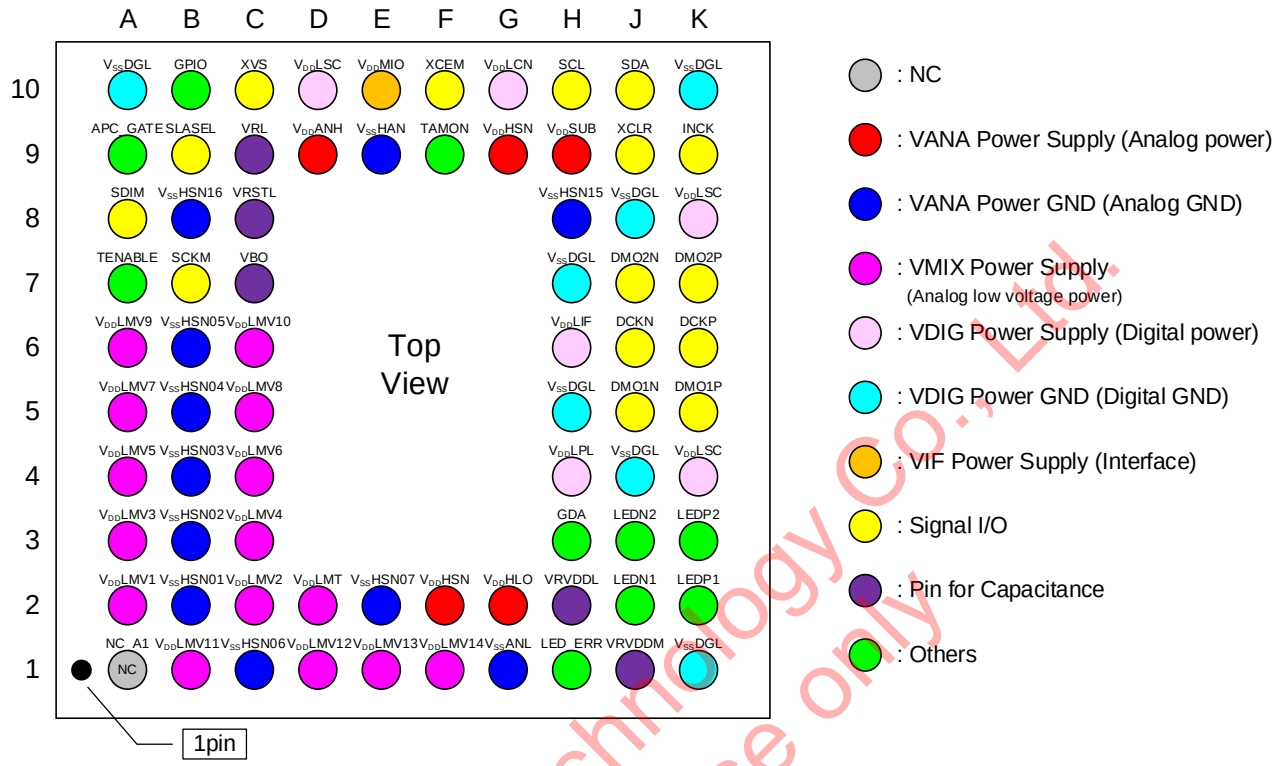
A B C D E F G H J K
10 9 8 7 6 5 4 3 2 1
VSSDGL GPIO XVS VDDLSC VDDMIO XCEM VDDLCN SCL SDA VSSDGL
APC_GATE SLASEL VRL VDDANH VSSHAN TAMON VDDHSN VDDSUB XCLR INCK
SDIM VSSHSN16 VRSTL VSSHSN15 VSSDGL VDDLSC
TENABLE SCKM VBO VSSDGL DMO2N DMO2P
VDDLMV9 VSSHSN05 VDDLMV10 VDDLIF DCKN DCKP
VDDLMV7 VSSHSN04 VDDLMV8 VSSDGL DMO1N DMO1P
VDDLMV5 VSSHSN03 VDDLMV6 VDDLPL VSSDGL VDDLSC
VDDLMV3 VSSHSN02 VDDLMV4 GDA LEDN2 LEDP2
VDDLMV1 VSSHSN01 VDDLMV2 VDDLMT VSSHSN07 VDDHSN VDDHLO VRVDDL LEDN1 LEDP1
NC_A1 VDDLMV11 VSSHSN06 VDDLMV12 VDDLMV13 VDDLMV14 VSSANL LED_ERR VRVDDM VSSDGL
NC
Top View
1pin
: NC
: VANA Power Supply (Analog power)
: VANA Power GND (Analog GND)
: VMIX Power Supply
(Analog low voltage power)
: VDIG Power Supply (Digital power)
: VDIG Power GND (Digital GND)
: VIF Power Supply (Interface)
: Signal I/O
: Pin for Capacitance
: Others

Figure 2 Pin Coordinates

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2. Pin Description

Table 1 Pin Description

No.	Pin No	Symbol	I/O	A/D	Description	Remarks
1	A1	NC_A1	—	—	N.C.	
2	A2	VDDLMV1	Power	A	VMIX power supply	
3	A3	VDDLMV3	Power	A	VMIX power supply	
4	A4	VDDLMV5	Power	A	VMIX power supply	
5	A5	VDDLMV7	Power	A	VMIX power supply	
6	A6	VDDLMV9	Power	A	VMIX power supply	
7	A7	TENABLE	I	D	Digital input	Leave this pin open (N.C.)
8	A8	SDIM	I/O	D	Digital I/O	Communication data input SDI of SPI Master
9	A9	APC_GATE	I/O	D	LDD enable output	
10	A10	VSSDGL	GND	D	VDIG GND	
11	B1	VDDLMV11	Power	A	VMIX power supply	
12	B2	VSSHSN01	GND	A	VANA GND	
13	B3	VSSHSN02	GND	A	VANA GND	
14	B4	VSSHSN03	GND	A	VANA GND	
15	B5	VSSHSN04	GND	A	VANA GND	
16	B6	VSSHSN05	GND	A	VANA GND	
17	B7	SCKM	O	D	Digital output	Communication clock output SCK of SPI Master
18	B8	VSSHSN16	GND	A	VANA GND	
19	B9	SLASEL	I	D	Digital input	I2C slave address select
20	B10	GPIO	I/O	D	LDD error detection flag input / XHS input / Test monitor output	
21	C1	VSSHSN06	GND	A	VANA GND	
22	C2	VDDLMV2	Power	A	VMIX power supply	
23	C3	VDDLMV4	Power	A	VMIX power supply	
24	C4	VDDLMV6	Power	A	VMIX power supply	
25	C5	VDDLMV8	Power	A	VMIX power supply	
26	C6	VDDLMV10	Power	A	VMIX power supply	
27	C7	VBO	Power	A	VANA power supply	Pin for Capacitance
28	C8	VRSTL	Power	A	VANA power supply	Pin for Capacitance
29	C9	VRL	Minus	A	Analog input	Pin for Capacitance
30	C10	XVS	I/O	D	Digital I/O / Test monitor output	Vertical sync signal
31	D1	VDDLMV12	Power	A	VMIX power supply	
32	D2	VDDLMT	Power	A	VMIX power supply	
33	D9	VDDANH	Power	A	VANA power supply	
34	D10	VDDLSC	Power	D	VDIG power supply	
35	E1	VDDLMV13	Power	A	VMIX power supply	
36	E2	VSSHSN07	GND	A	VANA GND	
37	E9	VSSHAN	GND	A	VANA GND	
38	E10	VDDMIO	Power	D	VIF power supply	
39	F1	VDDLMV14	Power	A	VMIX power supply	
40	F2	VDDHSN	Power	A	VANA power supply	
41	F9	TAMON	O	A	Analog output	Leave this pin open (N.C.)

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No.	Pin No	Symbol	I/O	A/D	Description	Remarks
42	F10	XCEM	O	D	Digital input	Communication enable XCE of SPI Master
43	G1	VSSANL	GND	A	VANA GND	
44	G2	VDDHLO	Power	A	VANA power supply	
45	G9	VDDHSN	Power	A	VANA power supply	
46	G10	VDDLCN	Power	D	VDIG power supply	
47	H1	LED_ERR	I/O	D	LDD error detection flag input	
48	H2	VRVDDL	Power	A	VMIX power supply	Pin for Capacitance
49	H3	GDA	I	A	Analog input	
50	H4	VDDLPL	Power	D	VDIG power supply	
51	H5	VSSDGL	GND	D	VDIG GND	
52	H6	VDDLIF	Power	D	VDIG power supply	
53	H7	VSSDGL	GND	D	VDIG GND	
54	H8	VSSHSN15	GND	A	VANA GND	
55	H9	VDDSUB	Power	A	VANA power supply	
56	H10	SCL	I/O	D	Digital I/O	Communication clock input/output of I2C
57	J1	VRVDDM	Power	D	VIF power supply	Pin for Capacitance
58	J2	LEDN1	O	D	Digital output	LVDS output (CLK -) for LED illumination signal
59	J3	LEDN2	O	D	Digital output	LVDS output (CLK -) for LED illumination signal
60	J4	VSSDGL	GND	D	VDIG GND	
61	J5	DMO1N	O	D	Digital output	MIPI output (DATA-)
62	J6	DCKN	O	D	Digital output	MIPI output (CLK-)
63	J7	DMO2N	O	D	Digital output	MIPI output (DATA-)
64	J8	VSSDGL	GND	D	VDIG GND	
65	J9	XCLR	I	D	Digital input	Clock clear
66	J10	SDA	I/O	D	Digital I/O	Communication data input/output of I2C
67	K1	VSSDGL	GND	D	VDIG GND	
68	K2	LEDP1	O	D	Digital output	LVDS output (CLK +) for LED illumination signal
69	K3	LEDP2	O	D	Digital output	LVDS output (CLK +) for LED illumination signal
70	K4	VDDLSC	Power	D	VDIG power supply	
71	K5	DMO1P	O	D	Digital output	MIPI output (DATA+)
72	K6	DCKP	O	D	Digital output	MIPI output (CLK+)
73	K7	DMO2P	O	D	Digital output	MIPI output (DATA+)
74	K8	VDDLSC	Power	D	VDIG power supply	
75	K9	INCK	I	D	Digital input	Clock input
76	K10	VSSDGL	GND	D	VDIG GND	

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3. Input / Output Equivalent Circuit

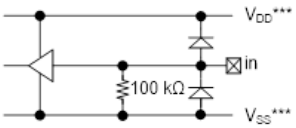
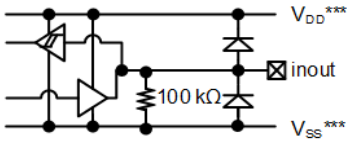
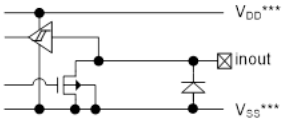
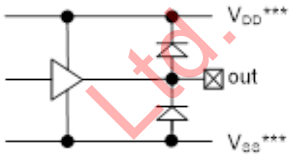
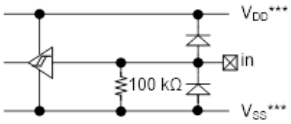
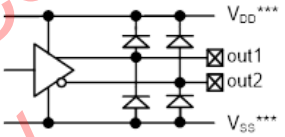
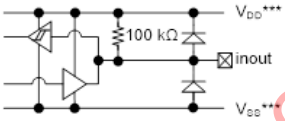
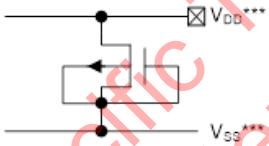
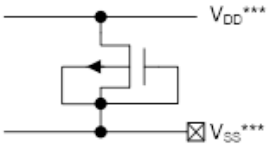
Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK XCLR		SDIM APC_GATE GDA	
SDA SCL		SCKM XCEM	
SLASEL		LEDP1 LEDN1	
XVS LED_ERR			
VDD***		VSS***	

Figure 3 Input/ Output Equivalent Circuit

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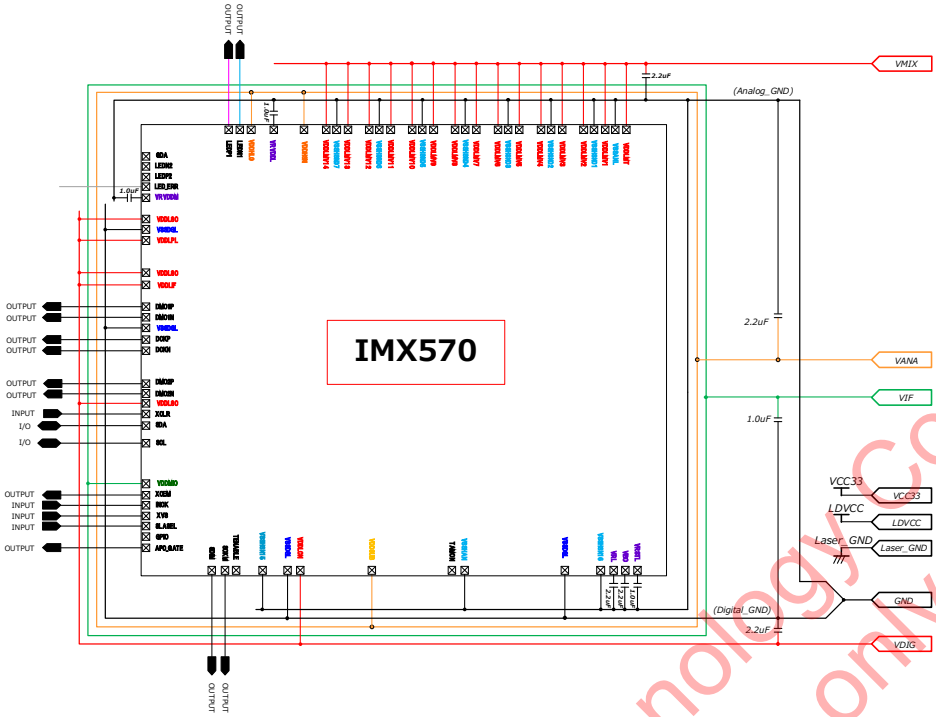
4. Peripheral Circuit Diagram

The following shows recommended application schematics.



	PAD No.	PAD name	Power	GND	Cap1[F]	Cap2[F]
High-Voltage power	33	VDDANH	2.8V	AGND	1.0uF	0.1uF
	40	VDDHSN			1.0uF	0.1uF
	44	VDDHLO			1.0uF	0.1uF
	45	VDDHSN			1.0uF	0.1uF
	55	VDDSUB			1.0uF	0.1uF
Low-Voltage power MIX	2	VDDLMV1	1.2V	AGND	1.0uF	0.1uF
	3	VDDLMV3			1.0uF	0.1uF
	4	VDDLMV5			1.0uF	0.1uF
	5	VDDLMV7			1.0uF	0.1uF
	6	VDDLMV9			1.0uF	0.1uF
	11	VDDLMV11			1.0uF	0.1uF
	22	VDDLMV2			1.0uF	0.1uF
	23	VDDLMV4			1.0uF	0.1uF
	24	VDDLMV6			1.0uF	0.1uF
	25	VDDLMV8			1.0uF	0.1uF
	26	VDDLMV10			1.0uF	0.1uF
	31	VDDLMV12			1.0uF	0.1uF
	32	VDDLMT			1.0uF	0.1uF
	35	VDDLMV13			1.0uF	0.1uF
	39	VDDLMV14			1.0uF	0.1uF
Low-Voltage power	34	VDDLSC	1.2V	DGND	1.0uF	0.1uF
	46	VDDLCN			1.0uF	0.1uF
	50	VDDLPL			1.0uF	0.1uF
	52	VDDLIF			1.0uF	0.1uF
	70	VDDLSC			1.0uF	0.1uF
	74	VDDLSC			1.0uF	0.1uF
Mid-Voltage power	38	VDDMIO	1.8V	DGND	1,0uF	
Other	27	VBO	2.8V	AGND	2.2uF	
	28	VRSTL	0V~1.8V		1.0uF	
	29	VRL	-1.2V		2.2uF	
	48	VRVDDL	1.2V		1.0uF	
	57	VRVDDM	1.8V	DGND	1.0uF	
	58	LEDN1	0V~1.8V		10pF	
	59	LEDN2	0V~1.8V		10pF	
	68	LEDP1	0V~1.8V		10pF	
	69	LEDP2	0V~1.8V		10pF	

Figure 4 Recommended Schematics

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5. Functional Description

5-1 System Outline

IMX570PLR-C is a Time-of-Flight (ToF) camera sensor which adopts the pixel architecture based on Current Assisted Photo Demodulator (CAPD) pixel with two tap shutter offers high responsivity, and high-speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, image binning circuit, timing control circuit for frame rate, CSI-2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions. Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data.

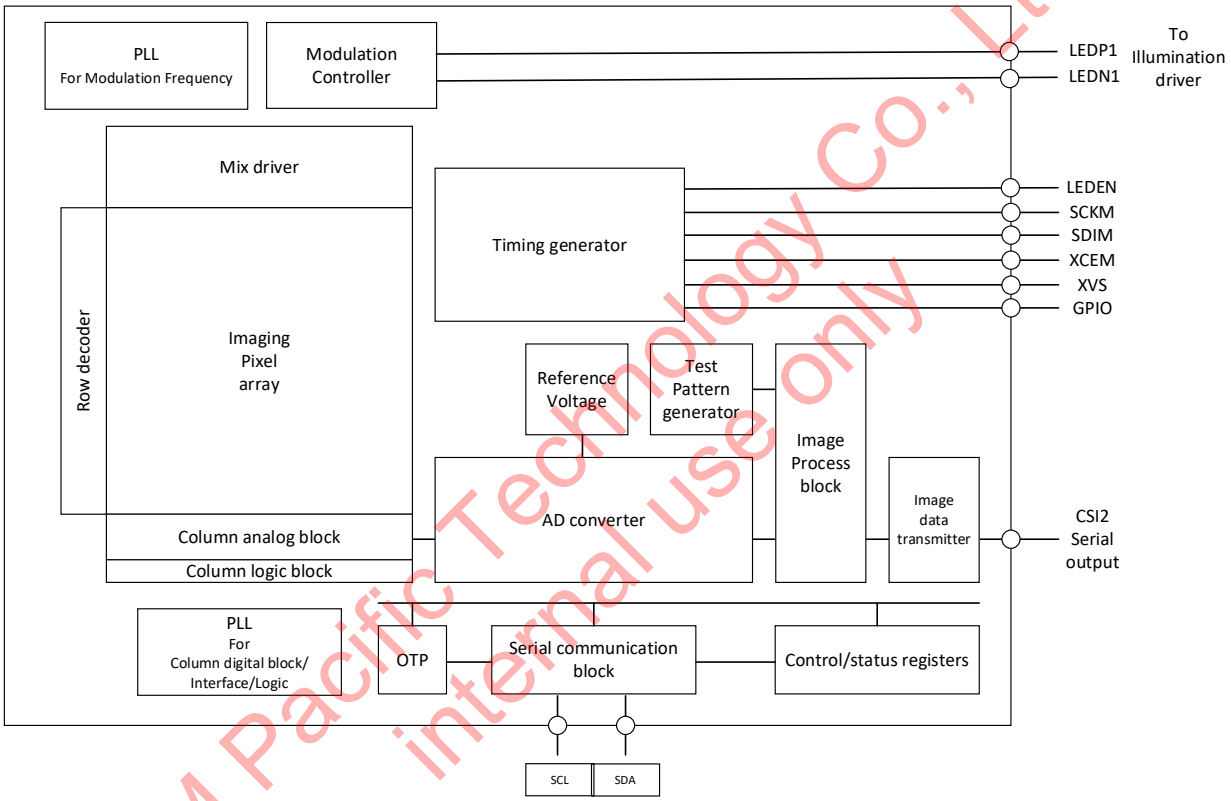

Figure 5 System Block Diagram

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5-2 Control Register Settings by Serial Communication

This sensor can use the 2-wire serial communication method for sensor control.
In this chapter, specification, method of 2-wire serial communication between the master device and this sensor is described.

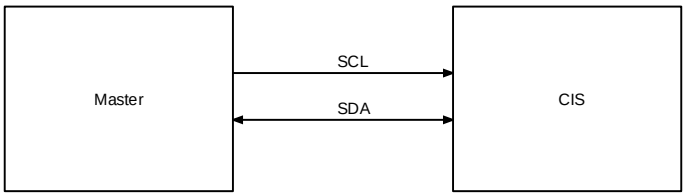

Figure 6 2-wire Serial Communication

5-2-1 I2C Communication Operation Specifications

The 2-wire serial communication method conforms to the camera control interface (CCI). CCI is an I2C Fast-mode Plus compatible interface, and the data transfer protocol is I2C standard.
This I2C serial communication circuit can be used to access the control-registers and status-registers of this sensor.

Table 2 Description of I2C Serial Communication Pins

Pin name	Description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of this sensor are mapped on the 16-bit address space. The register categories are shown below. Detail register information is shown in each chapter/section in this document and in Register Map.

Table 3 Abstract of Register Address Map for I2C Serial Communication

	Address range	Description	Note
I2C register	0x0000 - 0x7fff	Configuration register Read only and read/write dynamic register	
	0x8000 - 0xffff	Reserved	

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5-2-2 I2C Communication Protocol

The 2-wire serial communication method conforms to the Camera Control Interface (CCI). CCI is an I2C fast-mode
I2C serial communication supports a 16-bit register address and 8-bit data message type.

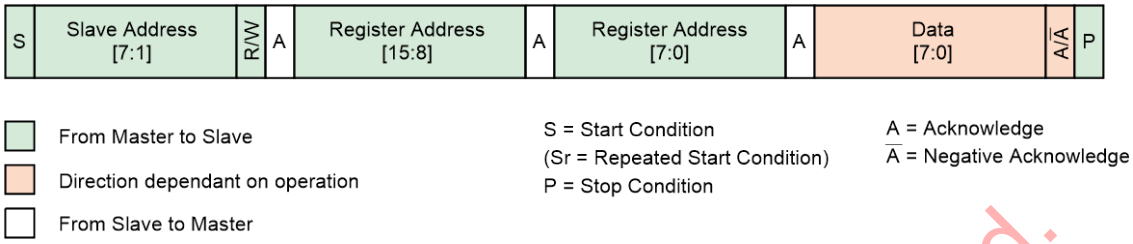
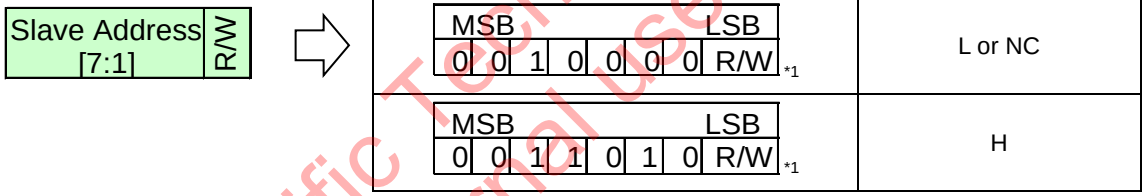


Figure 7 I2C Serial Communication Protocol

5-2-3 Default CCI Slave Address Configuration

5-2-3-1 First Slave Address

This sensor has a default Camera Control Interface (CCI) or 1st I2C slave address shown below. When called by this slave address, the serial communication interface is activated. Duplication of the address on the same bus must be prevented. This slave address is controlled by hardware connection of SLASEL pin.


Slave Address [7:1]
R/W
Slave Address (Read or Write)
* See Table4 for R/W bit
SLASEL (Pin B9)
MSB LSB
0 0 1 0 0 0 0 R/W *1
L or NC
MSB LSB
0 0 1 1 0 1 0 R/W *1
H

Note *1: R/W shows the direction of communication.

Figure 8 CCI (I2C) Slave Address

Table 4 R/W Bit

R/W bit	Direction of communication	Address
0	Write (master → sensor)	0: 0x20 or 0x34
1	Read (sensor → master)	1: 0x21 or 0x35

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5-3 Clock Generation and PLL

IMX570PLR-C equips embedded PLL to generate the necessary internal clocks and CSI-2 transmission clocks. Set the related registers according to the operation condition. See Software Reference Manual for more details of each function.

5-3-1 Clock System Diagram

IMX570PLR-C is equipped with 2 PLLs, one to 2 output clocks, IVTCK for image processing and IOPCK for MIPI output (PLL_VT in Figure 9), and the other to output IMXCK for pixel modulation signal (PLL_MX in Figure 9). PLL_VT can be set max 1440MHz ideally. PLL_MX can output 500 to 1200MHz. The both PLL based on a clock input with the 6 to 27 MHz range.
The both PLL could be configured with divider of up to 1/1 to 1/16 range, and multiply in the 16 to 511 range.

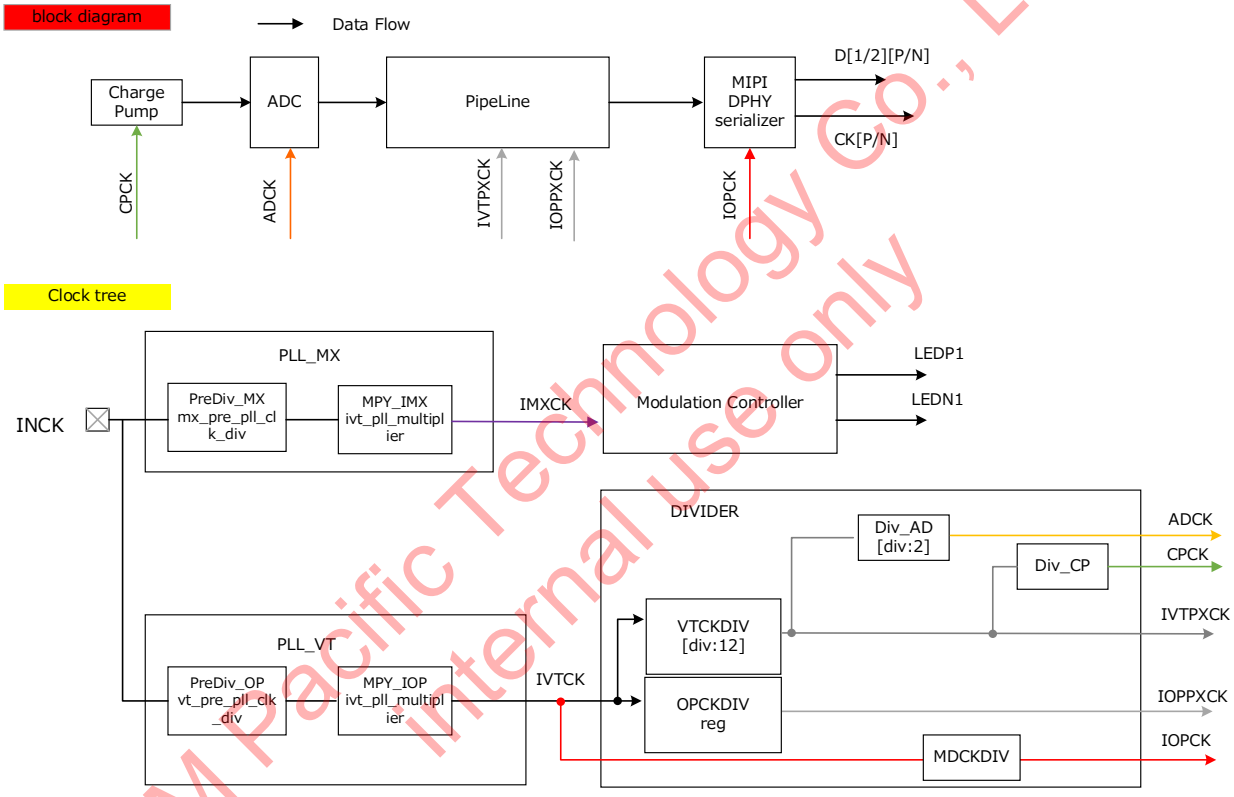

Figure 9 Clock System Diagram

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5-4 Image Readout Operation

This chapter describes relations between the imaging area, pixel readout orientation/readout and transmission frame/signal structure.
By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time and output format via I2C serial communication, this sensor outputs the image data.

5-4-1 Physical Alignment of Imaging Pixel Array (Top View)

Combination of Tap-A and Tap-B is counted as one pixel. Single data mode is defined as one pixel one data output. Dual data mode is defined as one pixel two data outputs.

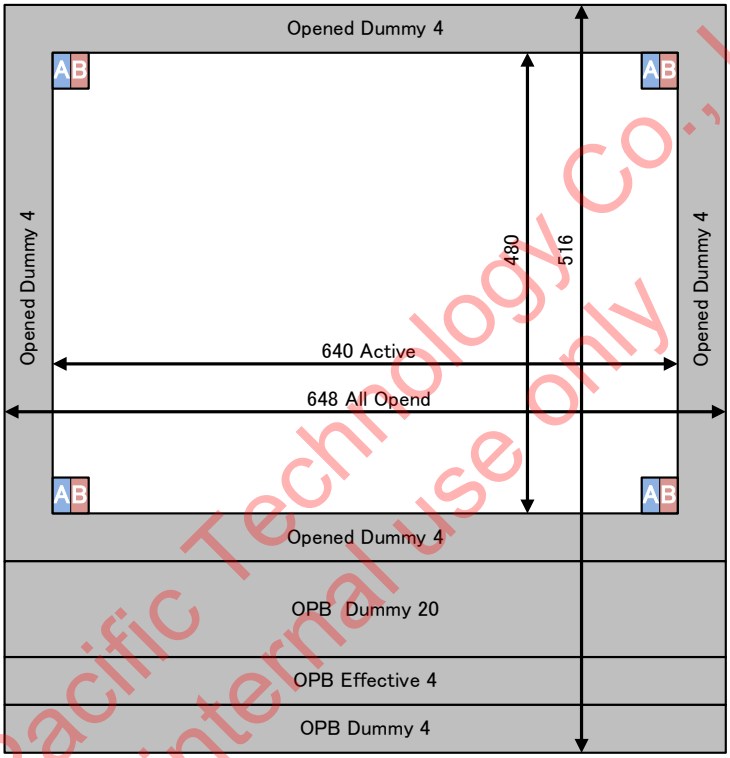

Figure 10 Physical Alignment of Imaging Pixel Array

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5-4-2 Order of Reading Image Data

Default readout direction is shown in the below figure.

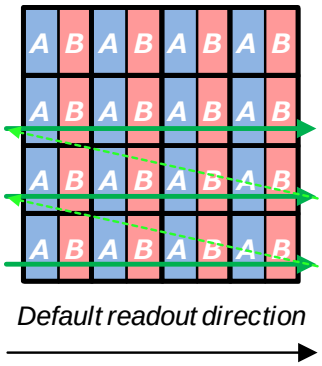

Figure 11 Readout Direction

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5-5 Output Image Format

This is the output image diagram of full pixel output mode. image data is output from the upper left corner of the diagram. The position of FS/FE can be set by register address 0x2c0c (FSFE_OUTPUT_CONTROL).

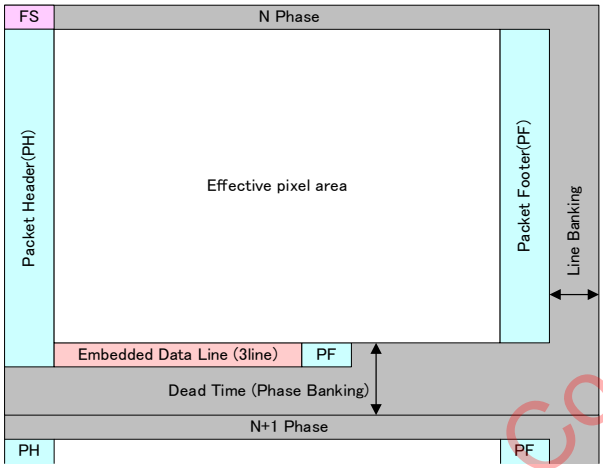

Figure 12 Full Pixel Output Mode Data Structure

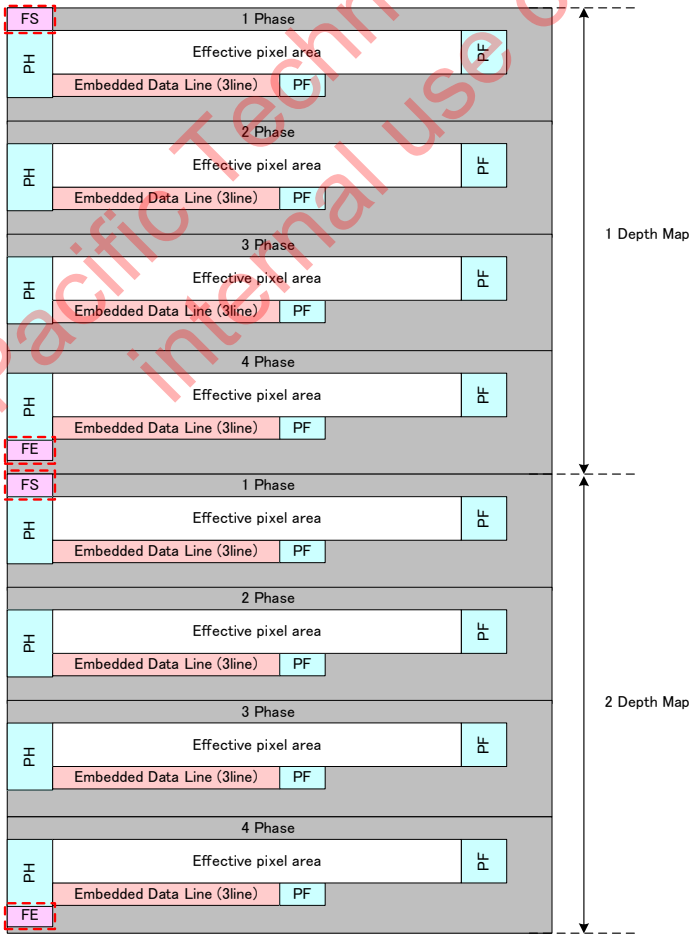

Figure 13 Frame End (FE) Output Data Structure (0x2c0ch = 1 (default))

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5-5-1 Image Size of Mode

IMX570PLR-C can capture and output full size or cropped image. Examples are shown in the below table. Definitions of each parameter are shown in the below figure.

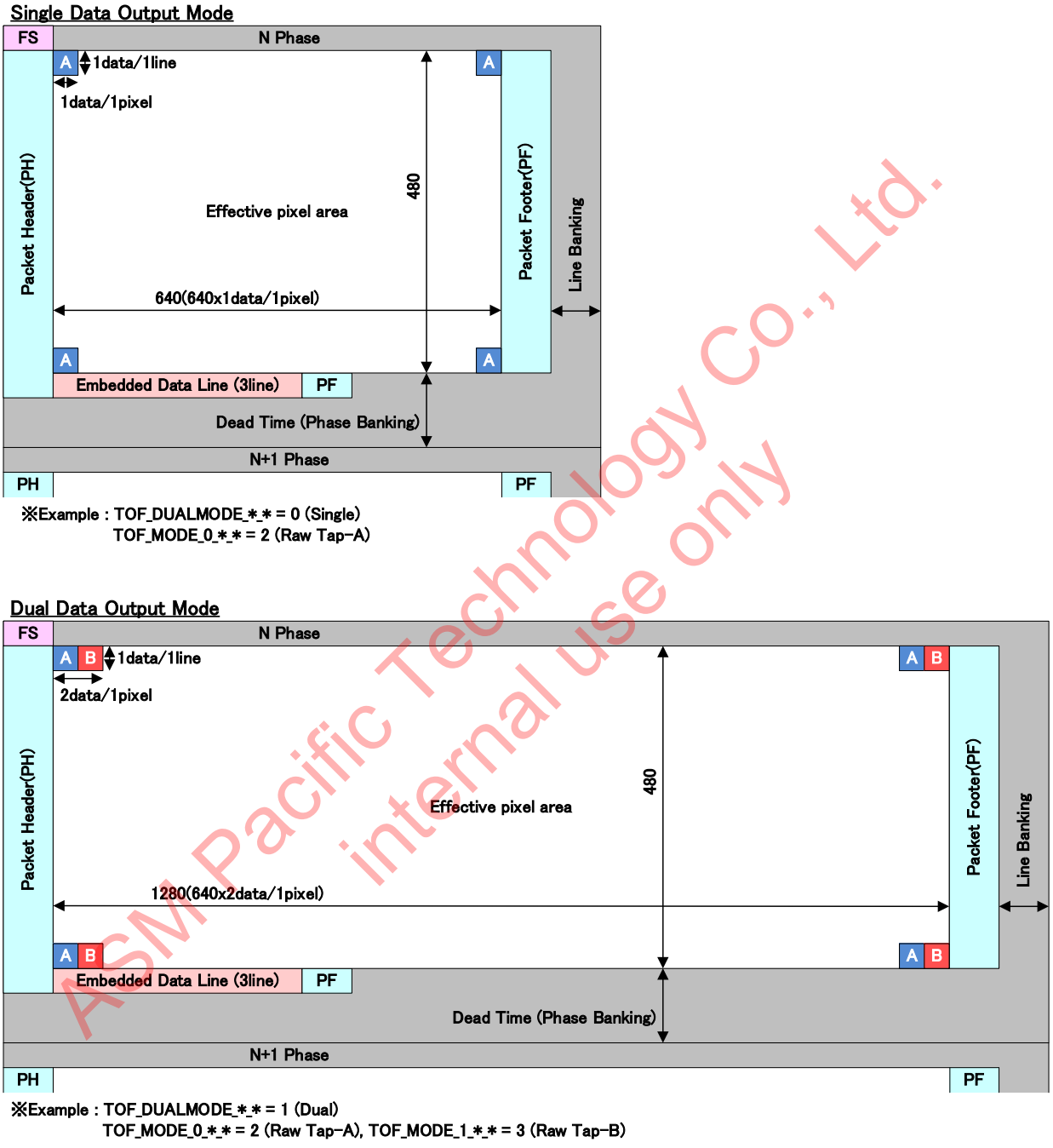

Figure 14 Image Size Parameter Definition

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Table 5 Modes and Image Sizes

		Modes			
		Full pixel No Binning Dual Data output mode		Full pixel No Binning Single Data output mode	
Number of vertical lines in imaging area		485		485	
Number of horizontal pixels in effective area		1280		640	
Number of lines and start position		Start position	Number of lines	Start position	Number of lines
Name of the	Frame start	1	1	1	1
	Number of vertical pixels in effective area	2	480	2	480
	Embedded data lines	482	3	482	3
	Frame end	485	1	485	1

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5-5-2 Description about Operation Mode

Main modes of this sensor are Full resolution and binning mode (2 × 2 or 4 × 4).

5-5-2-1 Image Size Related Settings

This sensor can output full size and/or re-sized images. Examples are shown in the below table.

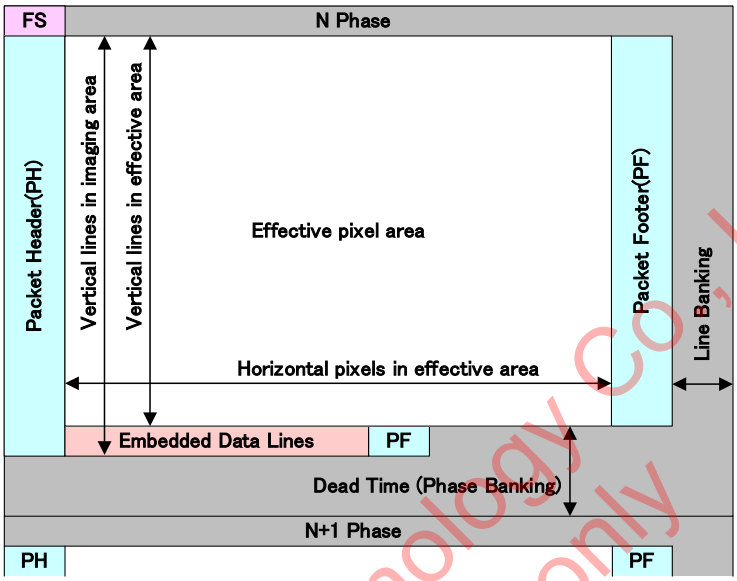

Figure 15 Image Size Parameter Definition

Table 6 Typical Image Output of Main Capture Modes

		Modes					
		Full resolution		2 × 2 Binning		4 × 4 Binning	
Number of vertical lines in imaging area		485		245		125	
Number of horizontal pixels in effective area		1280 or 640		640 or 320		320 or 160	
Number of lines and start position		Start position	Number of lines	Start position	Number of lines	Start position	Number of lines
Name of the areas	Frame start	1	1	1	1	1	1
	Number of vertical pixels in effective area	2	480	2	240	2	120
	Embedded data lines	482	3	242	3	122	3
	Frame end	485	1	245	1	125	1

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5-5-2-2 Normal Capture Mode Settings (full and binning)

This sensor can output full size and/or re-sized images. Examples are shown in the below figure.

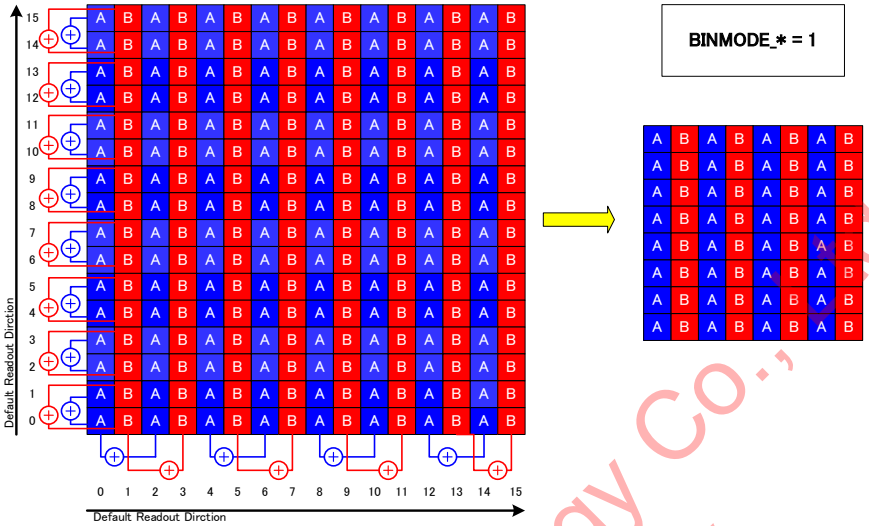

Figure 16 2 × 2 Binning

5-5-2-3 Image Size Related Functions

The relationships of image output size and the registers are shown below.

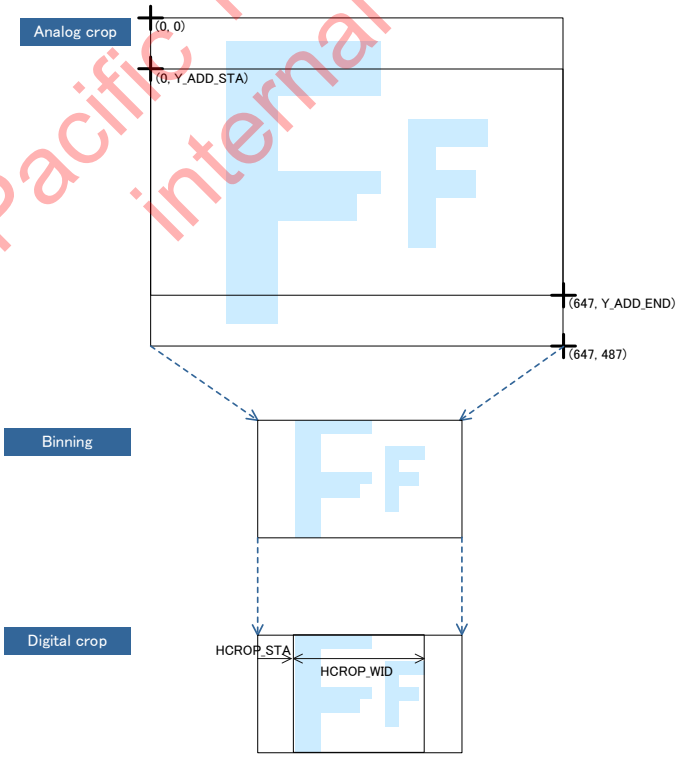

Figure 17 Image Size Related Functions

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Readout Start Position

Default readout position of IMX570PLR-C starts from the lower left when A1 Pin is placed at the upper right corner. Because the lens will invert the image both vertically and horizontally.

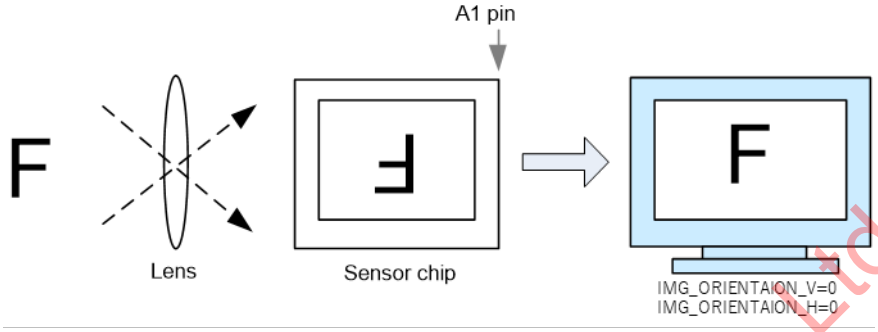

Figure 18 Readout Start Position

Vertical flip and horizontal mirror readout modes can be specified by IMG_ORIENTATION_V and IMG_ORIENTATION_H. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image.

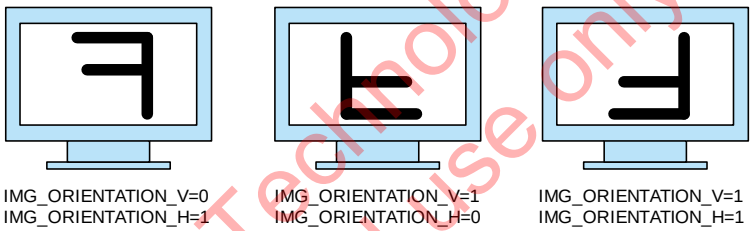

Figure 19 Readout Image for Each Combination of Flip and Mirror

5-5-3 Embedded Data Line Control

It is possible to output certain I2C serial register contents on max 3 lines just before the FE sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map.
See “IMX570 Software Reference Manual <4.5. Embedded data line control>”.

5-6 Image Signal Interface

5-6-1 MIPI Transmitter

This sensor outputs image signals by CSI-2 high speed serial interface consisting of one pair of clock lines and two pairs of data lines. Refer to MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) version 1.2 and MIPI Alliance Specification for D-PHY version 1.2 for details. Because signals are transmitted in differential pairs, impedance (generally 100Ω) between differential pairs near the receiver side during HS mode is required.

Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

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5-7 Modulation Pulse Generation

This sensor is equipped with embedded oscillator and PLL to generate the necessary internal clocks and CSI-2 transmission clocks. Set the related registers according to the operation conditions.
See “IMX570 Software Reference Manual <6.6. Modulation pulse generation>”.

5-7-1 Modulation Frequency Control

The pulse for pixel and light emission modulation is generated by dividing IMXCK into 1/8 to 1/240 frequency according to the word length of the CSI-2 interface.

5-7-2 Modulation Phase Control

The pulse for emitted light is controlled by IMXCK. The phase is defined by the delay difference between the pixel modulation signal and the light source signal. Regarding the phase setting, a register set consisting of A to C groups and 0 to 7 phase frames are prepared. The setting of the phase is determined by the modulation frequency and IMXCKDIV.

5-7-3 Variable Duty of the Illumination Signal

The light source pulse can set DUTY to a value other than 50%.

5-8 One-time Programmable (OTP) Memory

See “IMX570PLR-C OTP Manual”.

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6. How to Operate IMX570PLR-C

6-1 Power-on Reset

This sensor doesn't have a built-in "Power-on Reset" function.
The XCLR pin is set to "LOW" and the power supplies are brought up. Then the XCLR pin should be set to "High" after INCK supplied.

6-2 Power-on Sequence

6-2-1 Startup Sequence with I2C Serial Communication (external reset)

Follow the power supply start up sequence below.

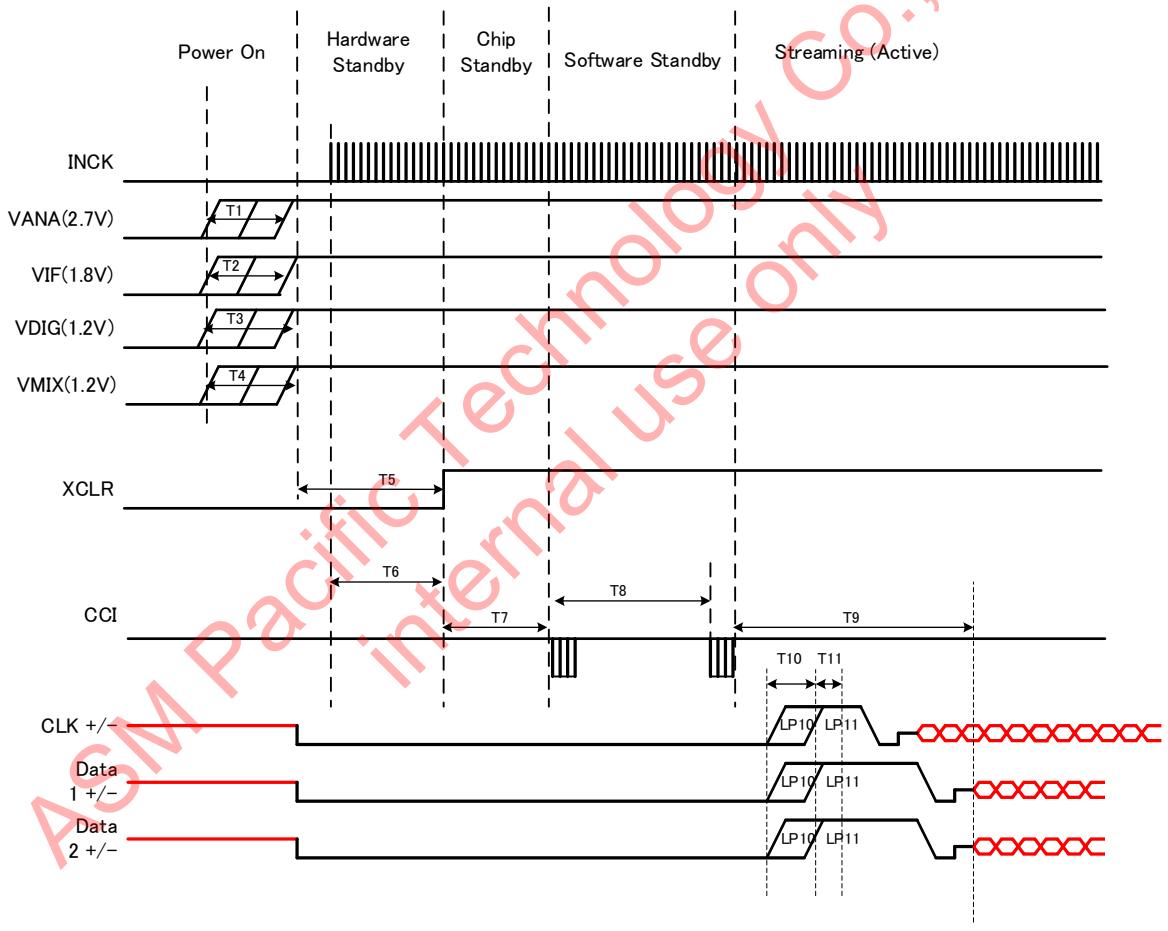

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Figure 20 Startup Sequence with I2C Serial Communication (external reset)

*Presence of INCK during Power-off is acceptable despite of above chart.

Table 7 Startup Sequence Timing Constraints (I2C serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA, VIF, VDIG and VMIX may rise in any order.		µs	Slew rate of VANA, VIF, VDIG and VMIX (0%-100%): Max. 50 mV/µs
VIF rising – VIF ON	T2			µs	
VDIG rising – VDIG ON	T3			µs	
VMIX rising – VMIX ON	T4			µs	
V rising – XCLR rising	T5	100	—	µs	Later T1, T2, T3 and T4
INCK start - XCLR rising	T6	0	—	µs	
I2C Read version ID register after XCLR rising	T7	1.0	—	ms	
Send Streaming Command wait time after XCLR rising	T8	12	—	ms	
(To complete reading all parameters from OTP)	T9	—	2.3	ms	
D-PHY power up	T10	1	1.1	ms	
D-PHY initialization period	T11	100	110	µs	

* XCLR needs to be Low level until all power supplies complete power-ON.

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6-3 Power-off Sequence

6-3-1 Power-off Sequence with I2C Serial Communication

Follow the power-off sequence below.

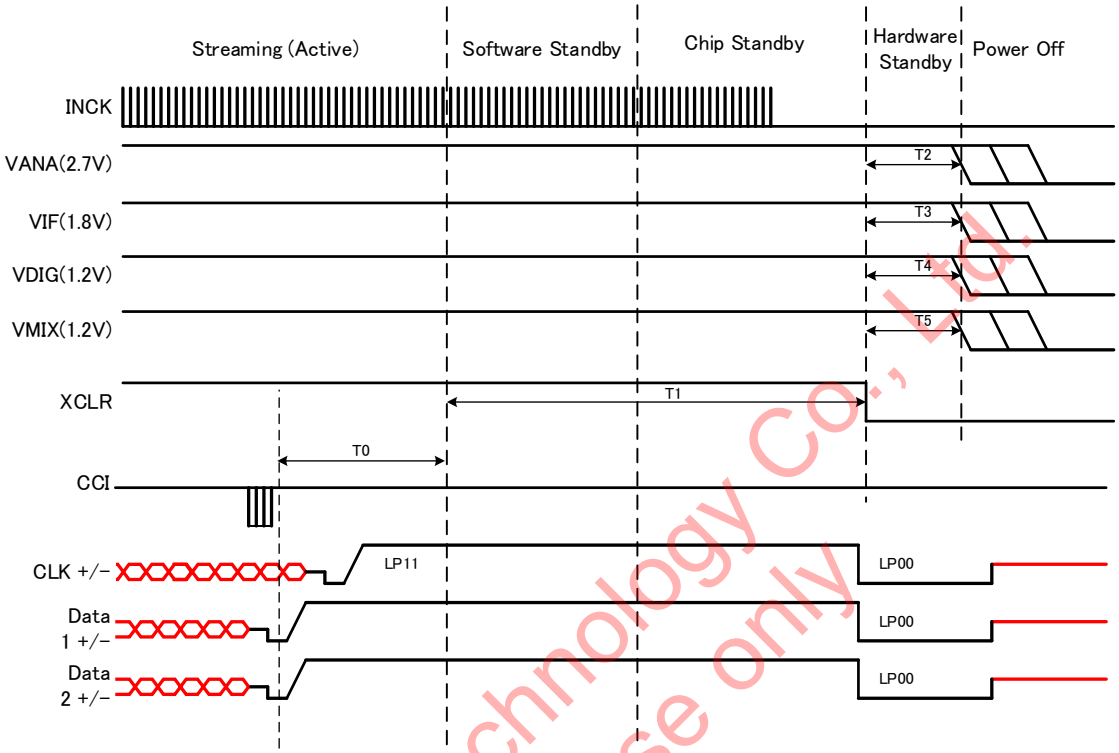

Figure 21 Power-off Sequence with I2C Serial Communication (external reset)

Table 8 Power-off Sequence Timing Constraints (I2C serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
Communication end – Software standby	T0	0	One frame time *1	s	
Software standby - XCLR negative edge	T1	0	—	µs	
XCLR Neg-edge - VANA, VIF, VDIG and VMIX falling	T2,T3,T4,T5	Min time = 0 (XCLR Neg-edge to power-off). VANA, VIF, VDIG and VMIX may fall in any order.		µs	

*1 One frame = Depth map unit

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7. Other Functions

See Application Notes for more details of each function.

7-1 Modulation Signal Adjustment

IMX570PLR-C has various adjustment functions for pixels and light emission signals.

7-1-1 Phase Adjustment (course)

IMX570PLR-C has course phase adjust function which is possible to adjust the relative delay of the modulation signal between the light source and the pixel signal in synchronization with the clock(IMXCKDIV).

7-1-2 Phase Adjustment (fine)

IMX570PLR-C has fine phase adjust function which is possible to adjust the relative delay of the modulation signal finer than course delay function.

7-1-3 Duty Adjustment

IMX570PLR-C has fine phase adjust function which is possible to adjust duty of modulation signal.

7-1-4 Thermal Meter

Internal temperature information can be read out from either register or embedded data.

7-2 Test Pattern Output (types of test patterns)

This sensor can output test patterns by using a built-in pattern generator.

7-3 Countermeasures for Laser Diode Driver(LDD) Abnormalities

Peripheral devices can output abnormality detection flag to IMX570PLR-C on LED_ERR pin. This abnormality detection flag can be received, and IMX570PLR-C can set LVDS to the standby state.
See **“**IMX570PLR-C Application Note <4 Countermeasures for Laser Diode Driver(LDD) Abnormalities>”.

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8. Electrical Characteristics

The Electrical Characteristics of the IMX570PLR-C is shown below

8-1 DC Characteristics

Table 9 DC Characteristics

Item	Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUB VDDHCM VDDHSN1,2,3 VDDHAN VDDHLO	VANA	2.6	2.7	2.9	V
	VDDLMT1,2 VDDLMV1 - 14	VMIX	0.79 *	1.2	1.3	V
	VRVDDL VDDLCN1,2,3 VDDLSC1 - 5 VDDLIF1,2 VDDLPL1,2	VDIG	1.1	1.2	1.3	V
	VDDMIO1,2 VRVDDM	VIF	1.7	1.8	1.9	V
Digital input voltage	SDA	VIH	0.7 × VIF	—	2.9	V
	SCL	VIL	-0.3	—	0.3 × VIF	V
Digital input voltage	XCLR, INCK, XVS, GPIO, LED_ERR	VIH	0.65 × VIF	—	VIF + 0.3	V
	SLASEL, SDIM, APC_GATE, GDA	VIL	-0.3	—	0.35 × VIF	V
Digital output voltage	SDA	VOH	VIF - 0.4	—	—	V
		VOL	—	—	0.4	V
Digital output voltage	XVS, GPIO LED_ERR SDIM, APC_GATE, GDA SCKM, XCEM	VOH	VIF - 0.4	—	—	V
		VOL	—	—	0.4	V

* Refer to 18-1

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8-2 AC Characteristics

8-2-1 Master Clock Waveform Diagram

8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

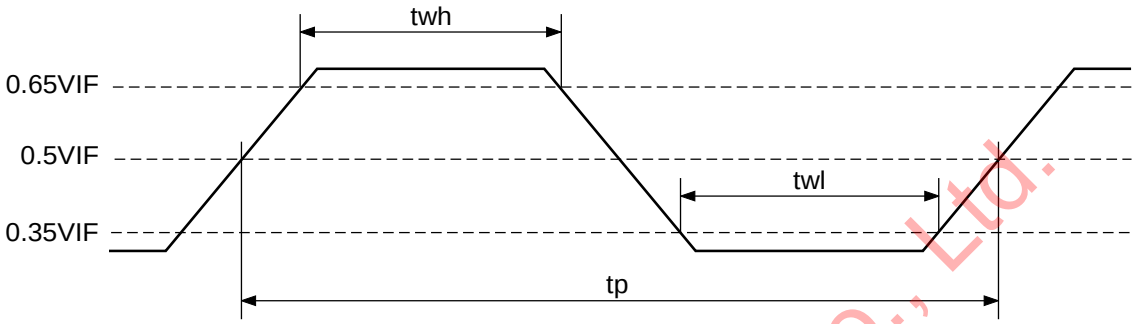

Figure 22 Master Clock Square Waveform Input Diagram

Table 10 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{SCK}	6	—	27	MHz
INCK clock period	t_p	37.0	—	166.7	ns
INCK low level width	t_{wl}	0.4 × tp	—	0.6 × tp	ns
INCK high level width	t_{wh}	0.4 × tp	—	0.6 × tp	ns
INCK jitter	Tjitter	—	—	600	ps

8-2-2 PLL Block Characteristics

Electrical characteristics of PLL block is shown below.

Table 11 PLL Block Characteristics

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0	—	27.0	MHz	
Input frequency range of phase comparator	6.0	—	12.0	MHz	
VCO frequency range(PLL_VT)	—	—	1440	MHz	
VCO frequency range(PLL_MX)	500	—	1200	MHz	
Output frequency range(PLL_VT)	—	—	1440	MHz	
Output frequency range(PLL_MX)	500	—	1200	MHz	
Settling time	—	—	1000	µs	

8-2-3 Definition of Settling Time of PLL Block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

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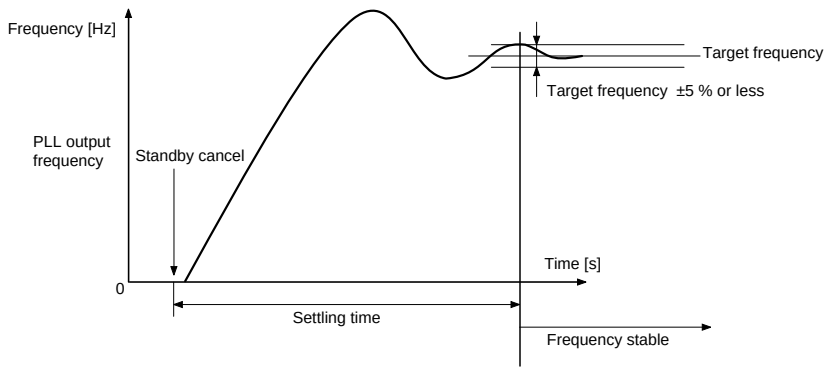

Figure 23 Definition of Settling Time

8-2-4 LVDS Characteristics

LVDS characteristics are shown below.

Table 12 LVDS Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
LVDS output voltage	LEDP LEDN	VCM	Low-voltage LVDS (termination resistance: 100 Ω)	—	VIF/2	—	mV
		VOD		100	150	200	mV

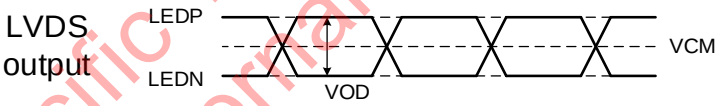

Figure 24 Low Voltage LVDS Output

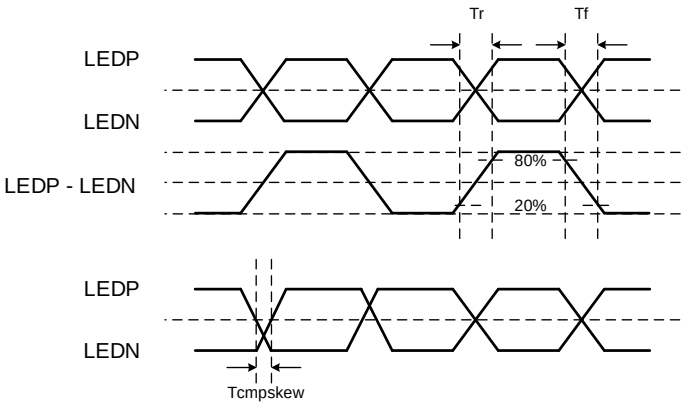

Figure 25 LVDS Characteristics

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Table 13 LVDS Specification

Serial Output (Output load capacitance: 4 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
clock duty	—	40	50	60	%
differential clock skew	Tcmpskew	—	—	50	ps
setup time	Tr	—	500	—	ps
hold time	Tf	—	500	—	ps

8-2-5 I2C Serial Communication Block Characteristics

I2C serial communication characteristics are shown below.

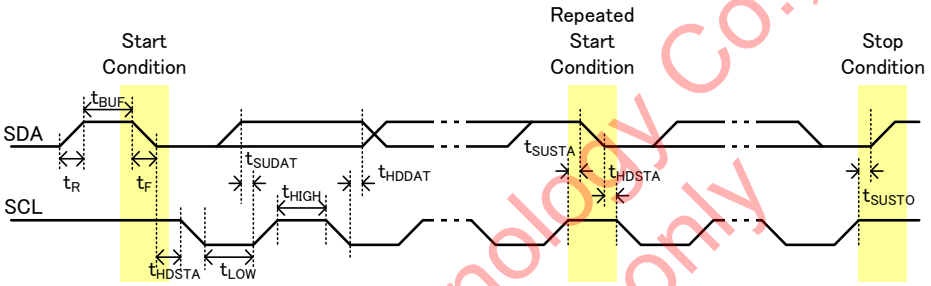

Figure 26 I2C Serial Communication Block Specification

Table 14 I2C Serial Communication Block Specification

Parameter	Symbol	Conditions	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
Low level input voltage	V_{IL}	—	-0.5	0.3 × VIF	V
High level input voltage	V_{IH}	—	0.7 × VIF	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V, Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V, Sink 3 mA	0	0.2 × VIF	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 × VIF→0.3 × VIF	—	250 (120)	ns
Input current	I_I	0.1 × VIF→0.9 × VIF	-10	10	µA
SDA I/O capacitance	$C_{I/O}$	—	—	10	pF
SCL Input capacitance	C_I	—	—	10	pF

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Table 15 I2C Serial Communication Block AC Specification

Parameter	Symbol	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
SCL clock frequency	f_{SCL}	0	400 (1000)	kHz
Rise time (SDA and SCL)	t_R	—	300 (120)	ns
Fall time (SDA and SCL)	t_F	—	300 (120)	ns
Hold time (start condition)	t_{HDSTA}	0.6 (0.26)	—	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6 (0.26)	—	µs
Setup time (stop condition)	t_{SUSTO}	0.6 (0.26)	—	µs
Data setup time	t_{SUDAT}	100 (50)	—	ns
Data hold time	t_{HDDAT}	0	—	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3 (0.5)	—	µs
Low period of the SCL clock	t_{LOW}	1.3 (0.5)	—	µs
High period of the SCL clock	t_{HIGH}	0.6 (0.26)	—	µs

Note) Fast-mode Plus supports only available with INCK ≥ 24.0MHz

8-2-6 Current Consumption and Standby Current

Table 16 Current Consumption and Standby Current

(30 depth frame/s, Single Frequency VANA = 2.7 V, VMIX = 1.2 V, VDIG = 1.2 V, VIF = 1.8 V, Tj = 60 ˚C)
(Full resolution, 30 depth frame/s, Modulation frequency: 120MHz, Integration time: 500µs, 4phase)

Item	Symbol	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}	12.4	16.4	mA	
Current consumption (mix)	I_{MIX}	64.1	83.4 (average value)	mA	
			1300 (integration time)	mA	<Note>
Current consumption (digital)	I_{DIG}	59.6	79.4	mA	
Current consumption (IF)	I_{IF}	2	3	mA	
Standby current (analog)	I_{STBANA}	—	10	µA	XCLR: Low fixed INCK: stop SLASEL=NC or Low
Standby current (mix)	I_{STBMIX}	—	83	µA	XCLR: Low fixed INCK: stop SLASEL=NC or Low
Standby current (digital)	I_{STBDIG}	—	9	mA	XCLR: Low fixed INCK: stop SLASEL=NC or Low
Standby current (IF)	I_{STBIF}	—	3	µA	XCLR: Low fixed INCK: stop SLASEL=NC or Low

Note) When under the following conditions and integration time, peak value is “1500[mA]”
(Full resolution, 30 depth frame/s, Modulation frequency: 120MHz, Integration time: 1000µs, 4phase)
(VANA = 2.8 V, VMIX = 1.3 V, VDIG = 1.3 V, VIF = 1.9 V, Tj = -10 ˚C to 60 ˚C)

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9. Spectral Sensitivity Characteristic

(Excludes neither lens characteristics nor light source characteristics.)

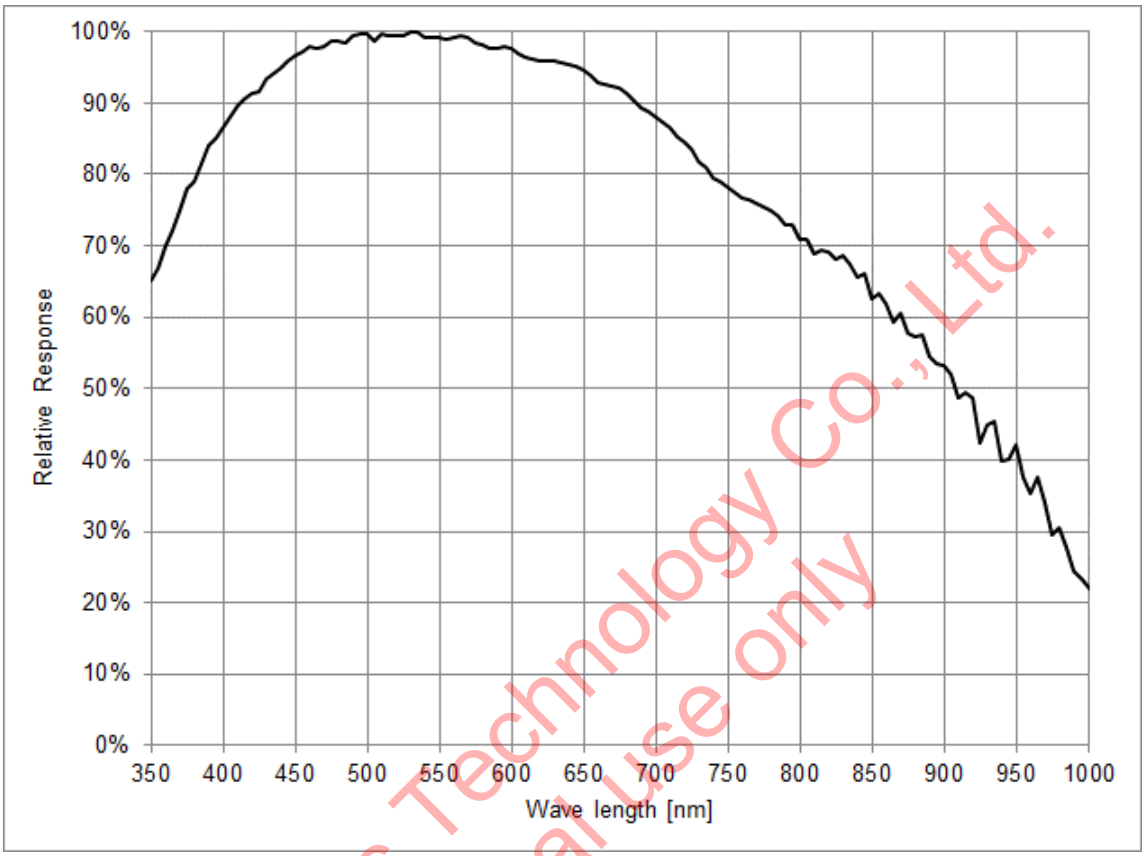

Figure 27 Spectral Sensitivity Characteristics

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10. Sensor Characteristics

10-1 Sensor Characteristics

Table 17 Sensor Characteristics

(30 depth frame/s, 940nm, VANA = 2.7 V, VMIX=1.2 V, VDIG = 1.2 V, VIF = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Dark signal	Vdt	—	—	15	LSB	Zone2D	11-3-1	
DC contrast	Cmod	72.5	—	—	%	Zone2D	11-3-2	
Saturation signal	Vsat	1012	—	—	LSB	Zone2D	11-3-3	

10-2 Zone Definition Used for Specifying Sensor Characteristics

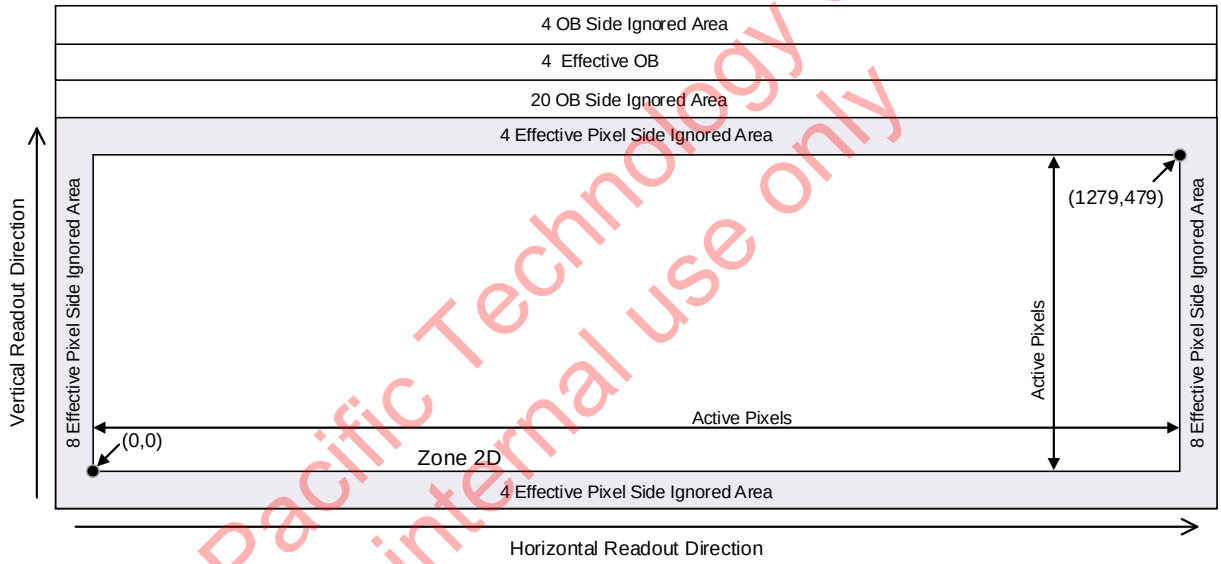

Figure 28 Zone Definition Diagram

Note: “ZONE2D” area is guaranteed the pixel performance.

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11. Measurement Method for Sensor Characteristics

11-1 Measurement Conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 18 Measurement Conditions

Supply voltage	VANA = 2.7 V, VDIG = 1.2 V, VMIX = 1.2 V, VIF = 1.8 V
Clock	INCK 24 MHz

11-2 Definition of Standard Imaging Conditions

11-2-1 Standard Imaging Condition I

Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

11-2-2 Standard Imaging Condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or integration time control by the electronic shutter.

11-2-3 Standard Imaging Condition III

Use light source is IR wavelength 940nm as a subject. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or integration time control by the electronic shutter.

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11-3 Measurement Method

11-3-1 Dark Signal

Measure the output difference between 6 [ms] signal output (Va) and 1 [ms] signal output (Vb) at the device in the light-obstructed state, and calculate the signal output at 5 [ms] storage by them using the following formula. Then, this is Vdt [LSB].

$$Vdt = (Va - Vb) \text{ [LSB]}$$

11-3-2 DC Contrast

Set the measurement condition to the standard imaging condition III. After adjusting the luminous intensity so that the average value of signal outputs is 520 [LSB] after subtracting dark level. Measure the number of electrons collected at proper position for each of Tap-A (Q1) and Tap-B(Q2), and substitute the values into the following formula for each case of Tap-A (Q1) and Tap-B (Q2).

$$Cmod = (Q1 - Q2)/(Q1 + Q2)$$

11-3-3 Saturation Signal

Set the measurement condition to the standard imaging condition III. After adjusting the luminous Intensity to 12 times the intensity with the average value of signal outputs after subtracting dark level, 520 [LSB], measure the average value of the pixel signal outputs.

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12. CRA Characteristics of Recommended Lens

12-1 Target CRA

The following figure and table show the target CRA (chief ray angle) of IMX570PLR-C.

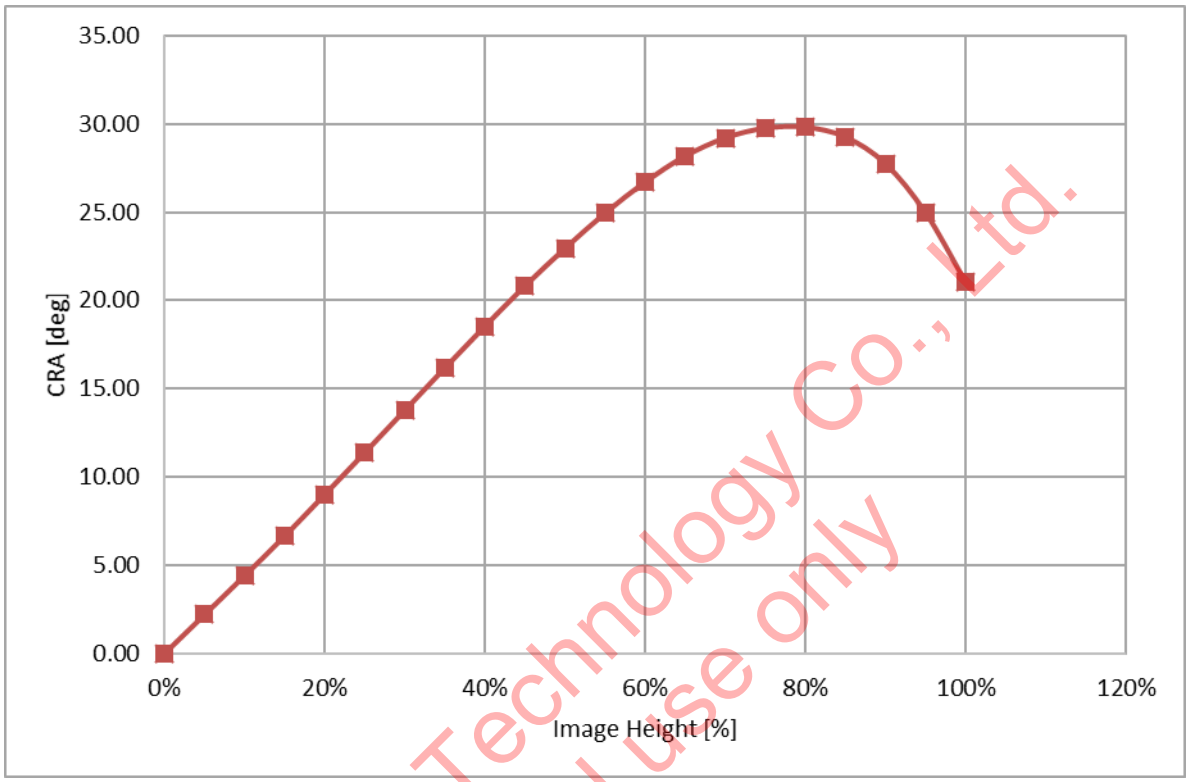

Figure 29 Target CRA of IMX570PLR-C

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13. Spot Pixel Specification

13-1 Spot Pixel

Table 19 Spot Pixel Specifications

(VANA = 2.7 V, VDIG = 1.2 V, VMIX = 1.2 V, VIF = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone				Measurement method	Remarks
		Zone 2D	Zone 3	Ineffective OB	Effective OB		
Black or white pixels at high light	30% ≤ D	1536 (pixel)	No evaluation criteria applied			13-2	
White pixels in the dark	268LSB ≤ D		No evaluation criteria applied			13-2	1ms integration time
Continuous Black or white pixels at high light	30% ≤ D	71 (pair)	No evaluation criteria applied			13-2	
Continuous White pixels in the dark	268LSB ≤ D		No evaluation criteria applied			13-2	1ms integration time

Note) 1. D...Spot pixel level.
2. Continuous pixels in the horizontal or vertical direction are rejected.

13-2 Single Defect Pixel

The following figure shows spot defect pixel. One pixel has two storage nodes and can output both through MIPI if register set to Dual Data output mode. Either A or B, or both are counted as 1 defect. Defects are either under “Black or white pixels at high light” or “White pixels in the dark”.

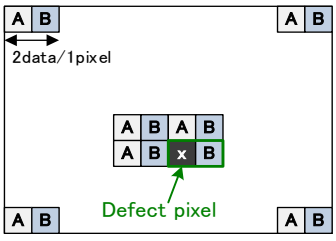

Figure 30 Spot Defect Pixel

Continuous pixels in the horizontal or vertical direction or oblique direction are described into following figures. Continuous defects are either under “Black or white pixels at high light” or “White pixels in the dark”. Either any pairs of “X” position defect and either A or B or both are counted as 1 pair defect pixel.

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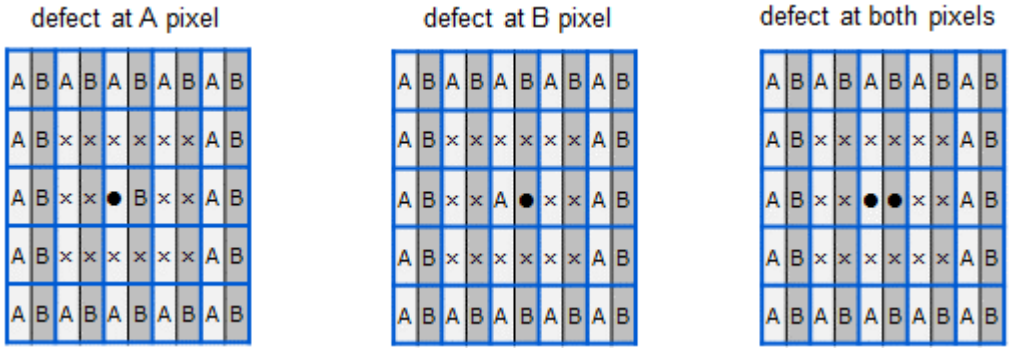

Figure 31 Continuous Spot Defect Pixel

13-2-1 Black or White Pixels at High Light

After adjusting the average value of the pixel signal output to 520 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the pixel A/B signal output Vx (x = A/B), and substitute the values into the following formula.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

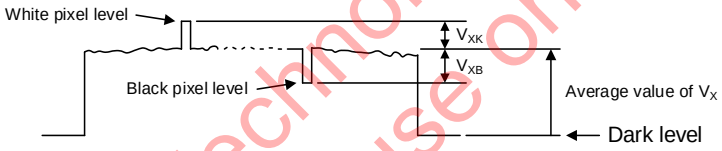

Figure 32 Measurement Method for Spot Pixels

13-2-2 White Pixels in the Dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

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14. Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	5.9 pcs
10.0 mV or higher	3.8 pcs
24.0 mV or higher	2 pcs
50.0 mV or higher	1.1 pcs
72.0 mV or higher	0.9 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

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15. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

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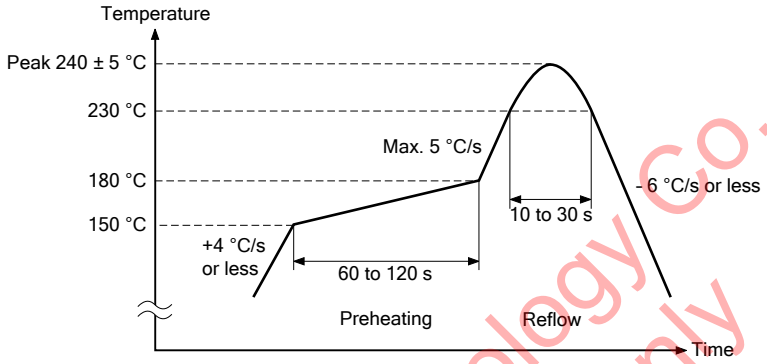
4. Reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Recommended temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.9

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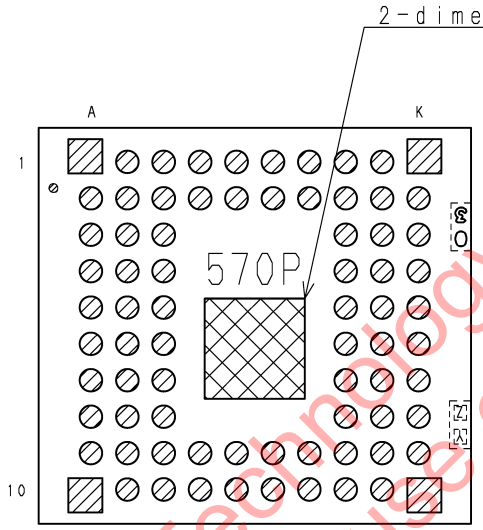
16. Marking



Note:Following characters enter into "Y", and"Z". (No Au coat)
Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-D570PLR(2D)

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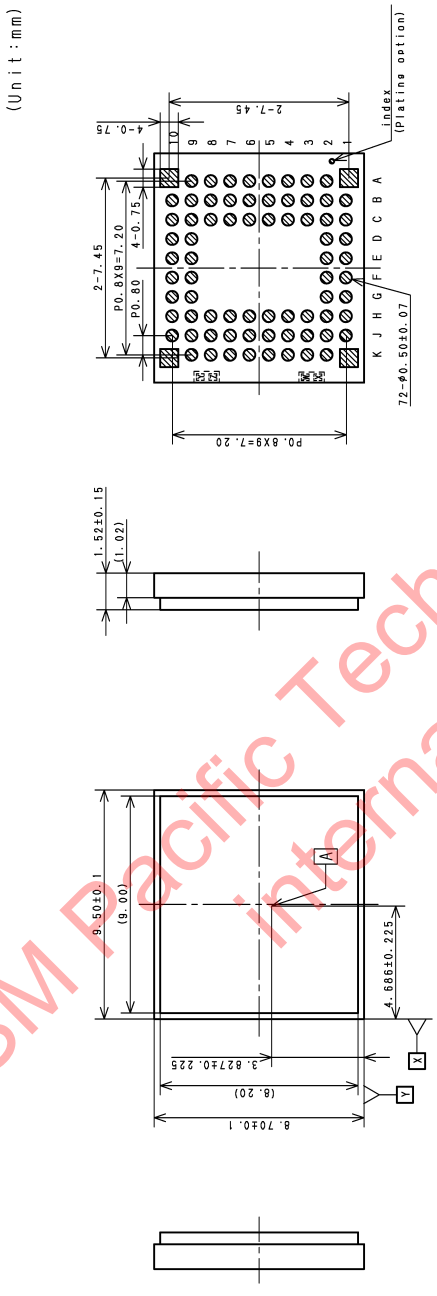
17. Package Information



1) " A " is the center of the effective image area
2) The rotation angle of the effective image area relative to " X " and " Y " is ± 1 °
3) The tilt of the effective image area relative to the height reference " Z " is less than 0.05 mm
4) The thickness of the cover glass is 0 . 5 mm
5) As for standard for resin overflow in package outside, it shall be accepted up to outermost line tolerance of package.
6) One character of alphabet or number shall be placed from W to Z part. (Plating option)

PACKAGE STRUCTURE

CLASSIFICATION	LGA
LEAD TREATMENT	GOLD PLATING
PIN NUMBER	76Pin
PACKAGE WEIGHT(Typ.)	0.29g
DRAWING NUMBER	AS-069(E)

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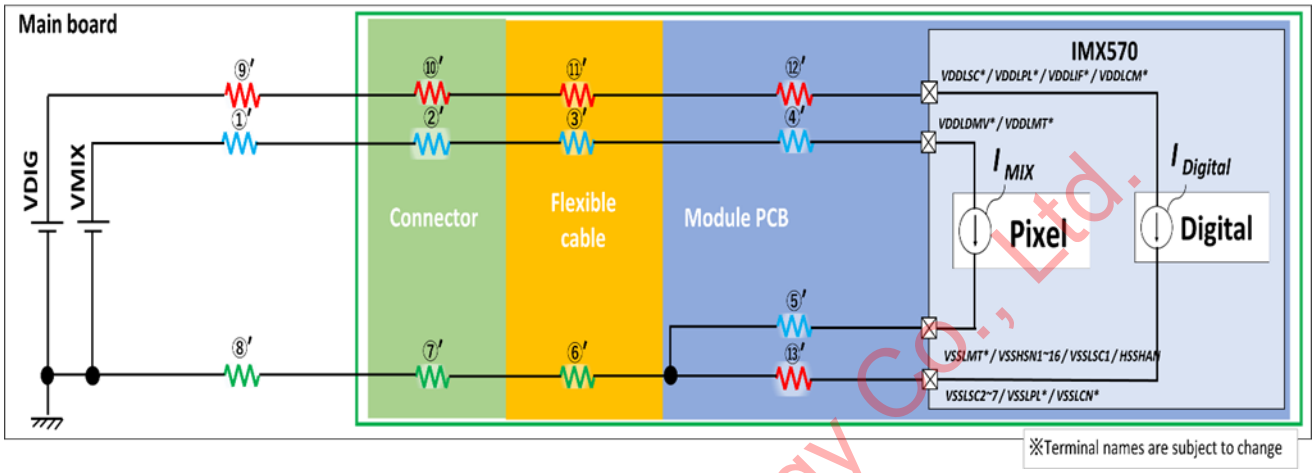
18. Appendix

18-1 Restrictions of Power Supply Condition

VDD_MIX and VDIG must be separated since the pixel modulation power supply consumes a huge current. And to marge AGND and DGND is recommended. Refer to the following restrictions.



	Impedamce @max
VMIX for VDDLMV* /VDDLMT*	①'+②'+③'+④'+⑤'+⑥'+⑦'<=180mohm
VDIG for VDDLSC* /VDDLPL* /VDDLIF* /VDDLCN*	⑥'+⑦'<=16mohm ⑨'+⑩'+⑪'+⑫'+⑬'+⑥'+⑦'+⑧'<=250mohm

Figure 33 Restrictions of Power Supply Condition

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